Semiconductor Monthly

Edited by Aimee Kalnoskas, Editor-In-Chief

Practical Applications of Current Limiting Diodes

by Sze Chin, Central Semiconductor Corp.

The current limiting diode (CLD) or current regulating diode (CRD) has been available since the early 1960's. Unfortunately, despite its simplicity and distinct advantages over conventional transistorized applications, it has seen only limited use. One reason may be designers' lack of familiarity with practical circuit design techniques involved with its use. Another reason may be that although many papers have been published on the device, most have dealt primarily with solid-state theory, rather than with practical applications. Therefore, it is the purpose of this paper to focus on how this device is used, rather than on what it is.

Conventional Constant Current Source vs. CLD

From basic circuit theory, an ideal current source is one with infinite output impedance. The term constant current source usually applies to a circuit that supplies a DC current whose amplitude is independent of a change in either load or supply voltage.

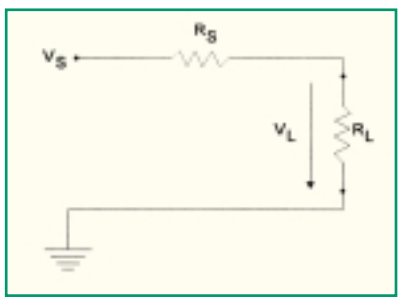

Fig. 1. Basic Constant Current Circuit

Basic Constant Current Circuit

The simplest circuit is a voltage source in series with a resistor as shown on Fig. 1. The current is $(V_S-V_L)/R_S$. The current would change very little if the load voltage, V_L, is small compared with the supply voltage, V_S, and the source resistance, R_S, is much larger than the load resistance, R_L. When the load voltage is in the order of several volts and accuracy within a few percent is required, the circuit in Fig.1 can be achieved only if V_S has a magnitude of several hundred volts. This may be feasible, but is impractical.

Transistor Constant Current Source

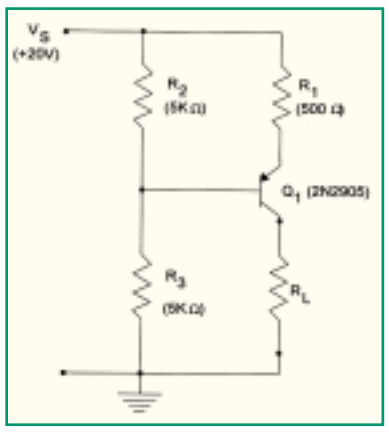

Fig. 2. Transistor Constant Current Circuit

For a constant current source, the use of a transistor as shown in Fig.2 would eliminate the need for a high voltage source. This circuit provides a constant current of approximately 10 mA, which is determined by the current through R_1, and in turn on the voltage across R_2, i.e. $V_S*R_2/[(R_2 + R_3)R_1]$. Since $I_{R1}=I_E=I_C=I_L$, The load current, I_L, is also $V_S*R_2/[(R_2 + R_3) R_1]$. This current will maintain its constant amplitude provided the transistor is not saturated, i.e. $V_L < V_s*R_3/(R_2+R_3)$.

As the load, R_L, changes, the collector voltage of Q_1 will change, but the collector current will change very little because its dynamic impedance, r_c, is very large, typically at 1 MΩ. The transistor operates like a current source with resistance, r_c. A non-transistor source would require a supply in the range of hundreds of volts to equal this performance.

Even though the Fig. 2 circuit represents a great improvement over that of Fig. 1, there are still limitations on its performance, such as temperature drift associated with both resistor and transistor parameters, notably the V_{BE} and the leakage I_{CO}. Also, any variation of V_S will cause a change in the bias voltage; therefore, will affect the constant current.

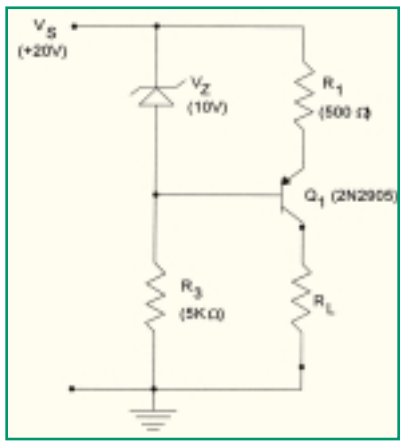

Fig. 3. Stabilized Current Source Circuit

Stabilized Current Source

Fig. 3 shows a stabilized version of the Fig. 2 circuit. In this circuit, a zener diode replaces R_2 of Fig. 2. The zener is equivalent to a battery in series with a low resistance, R_Z, which is typically 20Ω. This current has great stability against variation in the supply voltage, V_S. In the Fig. 2 circuit, 50 percent [$R_2/(R_2 + R_3)$] of the change in V_S would affect the Q_1 bias, whereas in the Fig. 3 circuit, only 0.04 percent [$R_Z/(R_Z + R_3)$] of a V_S change is felt on the Q_1 bias .

A low temperature coefficient zener may be used in this circuit. Many zeners with temperature coefficients of + 0.1%/°C or less are available. To further improve stability against temperature drift, a diode may be added in series with the zener, thus compensating for the V_{BE} drift.

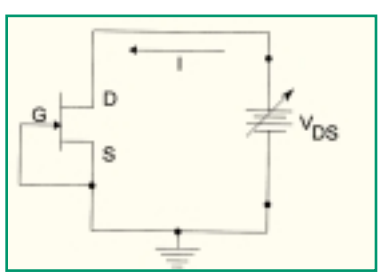

Fig. 4a. FET Constant Current Source Characteristics

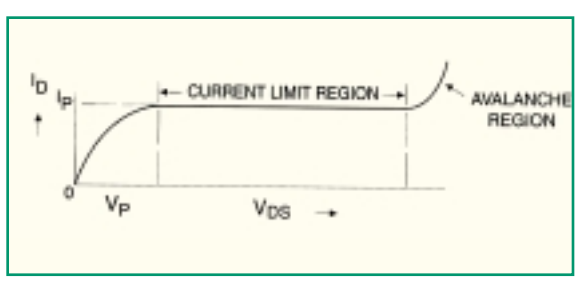

Fig. 4b. CLD Volt-Ampere

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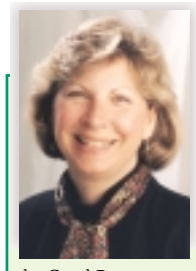


Silicon Valley Direct

Spring Products

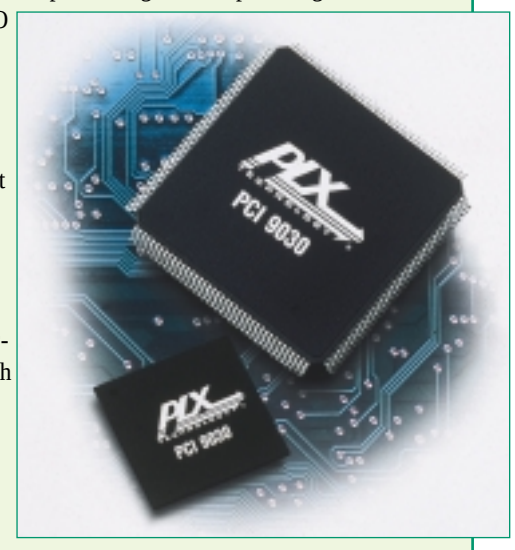
by Carol Rosen, Western Regional Editor

Semiconductor designers have been busy designing and developing a host of new ICs to speed systems, lower power or make building a system easier and less costly. As the IC economic picture continues to improve, capacity for most lines (with the exception of dynamic RAMs and some flash memories) is abundant although demand continues quite heavy.

Analysts expect that the spring and summer months will continue to be active with many IC makers getting new devices to market as quickly as possible in order to garner as much in sales as possible.

PLX Releases New Design Tools

PLX Technology, Inc. recently announced expanded design support for PCI- and CompactPCI-based products. The PCI 9030RDK-LITE and CompactPCI 9030RDK-LITE reference design kits simplify the development of PCI adapter designs incorporating PLX's PC9030 SMARTarget™ I/O accelerator.



PLX Technology recently announced two reference design kits for use with its PCI9030 chip.

The new tools each offer a basis for PCI and CompactPCI hardware and software development using the PCI9030. The kits also offer complete development environments to allow designers to migrate previous generation designs to those with PCI9030, including CompactPCI boards.

The kits include reference design boards and a PLX host software development kit (SDK). Each kit contains a PCI v2.2-compliant PCI board (PCI9030RDK-LITE) or CompactPCI board (CompactPCI9030RDK-LITE) based on the PCI9030 chip. The kits also offer comprehensive QFP/BGA/SSOP/TSOP/PLCC/SOIC footprints and prototyping area for developing, debugging and testing. Other features include up to 8 K × 32 dual-port SRAM, RS-232 serial port, six logic analyzer test headers, PLX option module connector, ISA connector footprint for designing PCI9030 into an ISA application and a CompactPCI form factor that is both 6U and 3U capable.

The tools also provide a hardware development kit CD-ROM containing all necessary hardware design information and documentation. They include a host SDK CD-ROM with Windows 98/2000/NT device drivers, PLXMon™ 2000 debugger with an EEPROM configuration screen and customizable hot links and comprehensive host API library and a sample PCI9030 chip.

Available this quarter, the PCI9030RDK-LITE is priced at $299 and the CompactPCI9030RDK-LITE is priced at $495, both with the PCI host SDK. ***PLX Technology, 390 Potrero Ave., Sunnyvale, CA 94086; (800) 759-3735; www.plxtech.com.***

Write in 1373 or www.ecnmag.com/info

Xilinx Offers PLDs in New Technology

Xilinx, Inc. recently announced new FPGAs fabricated in a new copper process technology. Xilinx and UMC Group have collaborated on copper interconnect technology for the last two years. That technology is the foundation for Xilinx's new Virtex™-E extended memory (Virtex-EM) FPGA.

Copper interconnect offers lower resistivity, minimizing power supply drop throughout the FPGA. The new family uses a 0.18 micron, six-layer metal process with the top two layers deploying copper interconnect. Those top layers are used to route clock lines to decrease clock and I/O skew for optimized performance.

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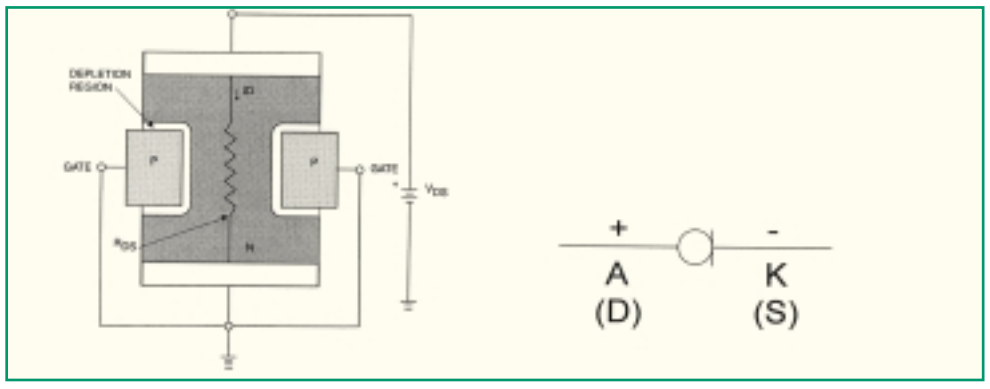

Figure 5a. Simplified Cross Section View of N-Channel FET

Figure 5b. CLD Symbol

Current Limiting Diode (CLD)

The CLD or constant current diode is basically a junction FET transistor operating with its gate shorted to the source terminal, as shown in Fig. 4a.

In this configuration, the JFET exhibits a unique current-limiting characteristic as V_{DS} is increased until the FET'S voltage breakdown limit is reached. This current-limiting characteristic is shown in Fig.4b. In order to explain the Fig. 4b characteristics, a cross section of the N-channel JFET is shown in Fig. 5a.

When the drain current begins to flow as voltage V_{DS} is applied, a voltage drop, V_{RDS}, is developed along the channel. This voltage drop provides a reverse bias on the PN junction between the gate and channel. Space charge or depletion regions are generated and spread into the channel. As V_{DS} is increased, the increase in current causes more reverse bias. Hence, the depletion regions grow until they meet, at which point any further increase in V_{DS} will be counter-balanced by an increase in the depletion region toward the drain. When this condition is reached, the current has reached its limiting condition. The V_{DS} voltage that causes the current to reach limiting condition is called V_P, the pinch-off voltage.

When a JFET is used as a CLD, its symbol becomes that shown in Fig. 5b. The drain becomes the anode, "A", and the source becomes the cathode, "K".

Because of its unique current-limiting characteristics, i.e. very large dynamic impedance (typically in the megohm range), and low temperature drift (as compared with the transistor), the CLD's advantages over transistors in current-limiting application are obvious. Moreover, a single CLD replaces five components in the transistorized version to achieve the same performance as a constant current source.

Market Availability Of CLD's

Today, CLD's are available with current ranges from 35 μA to 15 mA and associated impedance values from over 20 MΩ to several hundred KΩ. Their peak voltage rating ranges from 50 to over 100V. Temperature coefficients are typically within ±0.3%/°C. Near the 1 mA level, the T_C is close to 0% per °C. The low-cost CCL0035-CCL5750 series from Central Semiconductor has a current range from 35 μA to 6 mA, with peak voltage ratings of 100 V, and peak power at 600 mW in a DO-35 package. The CCLH080 - CCLH150 series, also in a DO-35 package, provides 6 mA to 15 mA, with a peak voltage rating of 50 V, and peak power of 600 mW. The use of CLD's is limited only by one's imagination in the application of the basic laws of electronics.

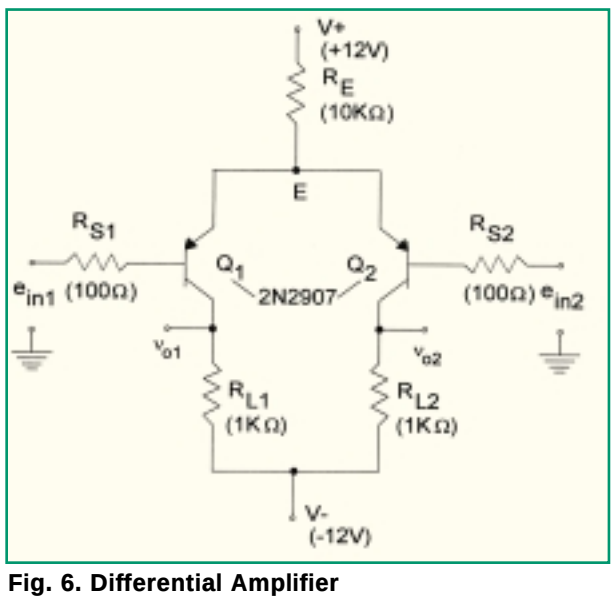

Fig. 6. Differential Amplifier

Differential Amplifiers

Today's most popular amplifier is the differential amplifier because, theoretically, it responds only to the difference of two signals, and is inherently temperature stable. The common-mode rejection ratio, CMR, is normally a measure of its performance — i.e. the higher the CMR, the better a device's performance. Presented in Fig. 6 is a standard differential amplifier circuit and in Fig. 7 is an AC equivalent circuit, which will be used to show how the CMR may be greatly improved by incorporating a CLD to provide a constant bias current.

To simplify the analysis, transistors Q_1 and Q_2 are assumed identical, $R_{S1} = R_{S2}$, $R_{L1}=R_{L2}$, and RE >>$(R_S/\beta + r_b/\beta + r_e)$. With $\boldsymbol{e}_{in1}$ present and $\boldsymbol{e}_{in2}$ shorted to ground, the signal, v_E, at terminal E would be 1/2 of $\boldsymbol{e}_{in1}$, since the impedances looking toward the emitters of Q_1 & Q_2 are the same. Hence

$v_E = 1/2\ \boldsymbol{e}_{in1}$. Therefore

$$\boldsymbol{i}_{E1} = (\boldsymbol{e}_{in1}. - v_E) = 1/2\ \boldsymbol{e}_{in1}. / [(r_e + (R_{b1} + R_{s1})/\beta_1)]$$

Since $vo_1 = -\boldsymbol{i}_{E1} R_{L1}$, the voltage gain

$$vo_1 / \boldsymbol{e}_{in1} = -1/2\ R_L/ [r_e + (r_{b1} + R_{S1})/\beta_1)]$$

For Q_2, since the emitter current is the same:

$$v_{o2} / \boldsymbol{e}_{in1} = +1/2\ R_L/ [r_e + (r_{b1} + R_{S1})/\beta_1)]$$

The voltage gain of Q_2 is the same as Q_1, but opposite in sign.

If the bias resistor, R_E, is finite, it has a parallel effect on the impedance ($r_e + r_b/\beta + R_S/\beta$) of Q_2. Hence v_E is changed from 1/2 $\boldsymbol{e}_{in1}$ to 1/2 $\boldsymbol{e}_{in1}$ [$R_E / (R_E + r_e + r_b/\beta + R_S/\beta$] and v_E thus is slightly smaller. Q_1's emitter current therefore is increased, and Q_2's emitter current is decreased. This implies that Q_1's gain is higher.

With regard to the source signal $\boldsymbol{e}_{in2}$, its effect is equal but opposite to that of $\boldsymbol{e}_{in1}$. Hence

$$v_{O2} / \boldsymbol{e}_{in1} = -1/2\ R_L/ [r_e + (r_b + R_S)/\beta]$$

$$v_{O1} / \boldsymbol{e}_{in2} = +1/2\ R_L/ [r_e + (r_b + R_S)/\beta]$$

With both $\boldsymbol{e}_{in1}$ and $\boldsymbol{e}_{in2}$ present, the output voltage can be shown by superposition to be:

$$v_{O1} = -1/2\ \boldsymbol{e}_{in1} \left(\frac{R_L}{r_e + [(r_b + R_S)/\beta]}\right) + 1/2\ \boldsymbol{e}_{in2} \left(\frac{R_L}{r_e + [(r_b + R_S)/\beta]}\right)$$

It follows that:

$$v_{O1} = 1/2 \left(\frac{(e_{in2} - e_{in1})\ R_L}{r_e + [(r_b + R_S)/\beta]}\right), \text{ and } v_{O2} = 1/2 \left(\frac{(e_{in1} - e_{in2})\ R_L}{r_e + [(r_b + R_S)/\beta]}\right)$$

The above shows that if $e_{in1} = e_{in2}$, then $v_{O1} = v_{O2} = 0$; and if $e_{in1} = -e_{in2}$, then the above becomes

$$v_{O1} = -e_{in1} \left(\frac{R_L}{r_e + [(r_b + R_S)/\beta]}\right), \quad v_{O2} = +e_{in2} \left(\frac{R_L}{r_e + [(r_b + R_S)/\beta]}\right)$$

The amplifier thus produces equal and opposite outputs based upon the difference between the two input signals, but independent of their sum.

If $e_{in1} = e_{in2}$, and R_E is finite, then the current in Q_1 and Q_2 is no longer constant, and a total change of e_{in1}/R_E results. Each transistor's current changes by 1/2 e_{in1}/R_E, with a resulting output change of -1/2 $e_{in1}\ R_L/R_E$, out of phase with e_{in1}. A finite R_E would result in appreciable output, even when $e_{in1} = e_{in2}$.

When a differential amplifier is used to measure the difference of two signals, the criteria for performance is the ratio of the gain due to the difference to the gain due to the sum of the two input signals, known as common mode rejection, or CMR.

$$CMR \approx \frac{V_{out}}{(e_{in1} - e_{in2})} \Big/ \frac{V_{out}.}{(e_{in1} + e_{in2})}$$

$$CMR \approx \frac{2\ R_E}{r_e + [(r_b + R_S)/\beta]} \approx \frac{2\ R_E.}{1/g_m + R_S/\beta]}$$

For the Fig. 6 circuit, $1/g_m \approx 50\Omega$, $\beta \approx 50$

Hence, $CMR = \frac{2\ (10K)}{50 + \frac{100}{50}} = 385.$

If a 1 mA CLD is used for R_E, as shown in Fig. 8 (page 52), and since the Z_d for such a CLD is typically 1 Meg Ω,

Then:

$$CMR = \frac{2(1{,}000{,}000)}{52} = 38{,}461$$

One can see the significant improvement in CMR by a factor of more than 100X with the CLD.

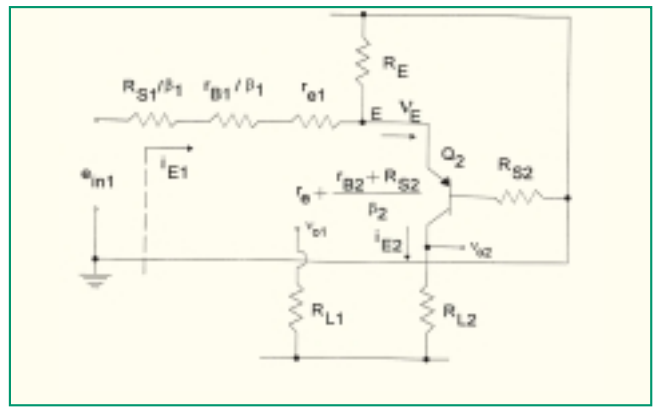

Fig. 7. Equivalent AC Circuit with $e_{in1} \neq 0$ & $e_{in2} = 0$

Current Amplification & Division

Even though the current range of the CLD is limited to less than 15mA, this current may be practically amplified to a higher level. Shown in Fig. 9 is a circuit using an op-amp to either amplify or attenuate a CLD's current level.

Since an ideal op-amp has infinite input impedance, its input currents IN+ and IN - are zero, and its differential input $V_{IN} = 0$. Therefore,

$$V_{R1} = V_{R2}$$
$$I_{R1}\ R_1 = I_{R2}\ R_2$$

Since IN- = 0, $I_{R1} = I_{CLD}$

And since IN+ = 0, $I_{R2} = I_{RL}$

Hence $I_{CLD}\ R_1 = I_{RL} * R_2$

$$I_{RL} = I_{CLD} \frac{R_1}{R_2}$$

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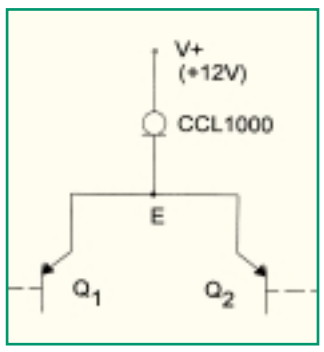

Fig. 8. CLD Replacing R_E

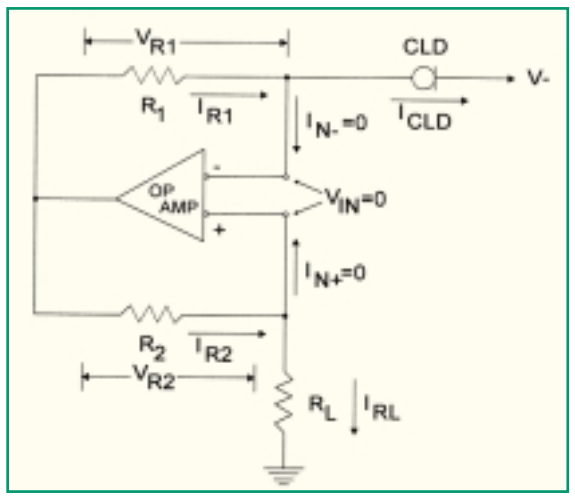

Fig. 9. Current Multiplying/Dividing Circuit

This shows that the CLD's current level may be amplified or attenuated by the ratio of resistors R_1 and R_2. The maximum load current is limited by the Op Amp's current capacity - i.e. for a given I_{RL}, the maximum R_L is limited by the input voltage rating of the Op Amp, such that I_{RL} R_L < max. input voltage rating.

There are many Op Amp's available with current ratings up to several hundred mA, and with input voltage ratings up to 15 V. Their input voltage offsets range from a few μV down to a few μV, and input offset currents from 1 μA down to less than 1 nA. Hence the use of a high performance Op Amp provides very accurate current amplification or attenuation. Assume, for example, that I_{CLD}= 1 mA, R_1 = 1K and R_2 =100. If R_1/R_2=10, then I_{CLD} is amplified 10 times, allowing 10 mA to the load. If the input offset were 1 μV, this would cause only a 0.1% error. And if the input offset current were 10 μA, this would still cause only a 0.1% error.

Resistance Measurement

The Current Amplifying/Dividing Technique shown above may be easily applied to resistance measurement. The measurement circuit, if digitally controlled and programmed, may become part of an automatic test equipment (ATE) system.

From the basic formula $V_X = IR_X$, the voltage, V_X, is proportional to the unknown resistance, R_X. If I is known, the unknown R_X may be found by reading the voltage V_X. Referring to the Fig. 9 circuit, if we select R_1 such that I_{CLD} x R_1 =1V, the voltage on R_2 is also 1V.

Hence $I_{R2}R_2 = 1V$
$I_{R2}R_x = V_X$
$R_X = R_2V_X$

If R_2 is selected in multiples of 10, and V_x is limited to 1V maximum, then the unknown, R_X, may be read directly on a decimal scale.

For example if R_2 is:

100 Ω, Rx = 100 Vx
1,000 Ω, Rx = 1,000 Vx
10,000 Ω, Rx = 10,000 Vx
100,000 Ω, Rx = 100,000 Vx
1,000,000 Ω, Rx = 1,000,000 Vx

The above shows that if the five resistor values from 100 Ω to 1MΩ are incorporated for R2, effectively the circuit of Fig. 9 is now transformed into a resistance-measuring circuit with 5 decimal scales capable of measuring resistances up to 1 MΩ in five ranges. Fig. 10 shows such a transformed circuit with discrete components and values.

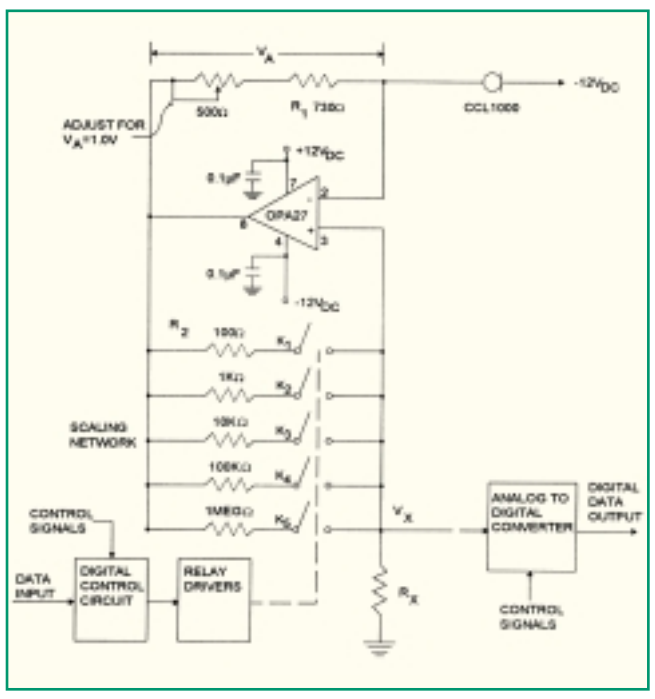

Fig. 10. Resistance Measuring Circuit

This circuit may be automated with an A-D converter to convert Vx into Digital Data. Selection of the proper scale may be achieved through auto-ranging techniques under digital control.

Voltage Amplitude Reference

When a known constant current flows through a known resistor, a known voltage is generated. This may be used as a reference (as shown in Fig. 11a) in many feedback control applications such as DC regulation, motor speed control, automatic frequency-control, and automatic gain-control. When the voltage reference is switched on and off, as shown on Fig. 11b, it becomes a pulse with a known reference amplitude, which can be used in a pulse-generator design.

Ultra High-Speed Pulse Amplitude

Shown in Fig. 12 is a high-speed pulse amplitude reference circuit. The amplitude of 1 volt is generated by a 10mA CLD through 100 ohms. The rise and fall times are less than 10 nS, achieved with the use of Schottky diodes as switches, driven by an ultra-high-speed op-amp.

In this circuit, the Op Amp, U_1, is driven by a digital TTL pulse signal. When the signal goes to logic "0", U_1's output goes high, and diode D_3 is reverse biased and turned off, thus allowing the constant current through diode, D_2, onto R_1. As the TTL signal goes high, U_1's output goes low, thus forward-biasing D_3 and reverse-biasing D_2. Hence, the current to R_1 is switched off. The result is a reference pulse with precision amplitude.

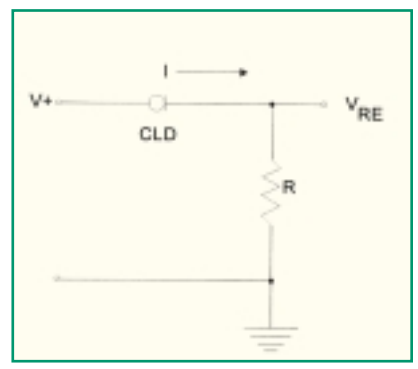

Fig. 11a. Voltage Reference

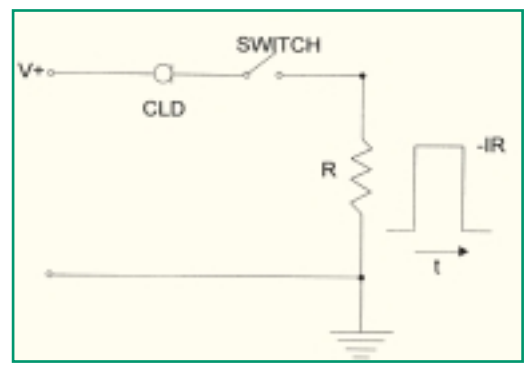

Fig. 11b. A Pulse Amplitude Reference

Other Applications

These are three versions of Ohm's law, namely:

$$v = iR, \quad i = C\frac{dv}{dt} \quad and \quad v = L\frac{di}{dt}$$

So far, only the v = iR version has been used in this presentation of practical applications. As for the other two versions, v =L di/dt is not relevant, since di/dt for a constant current device is zero. The remaining applicable equation is: i =C dv/dt. Presented next are some suggested uses of this formula.

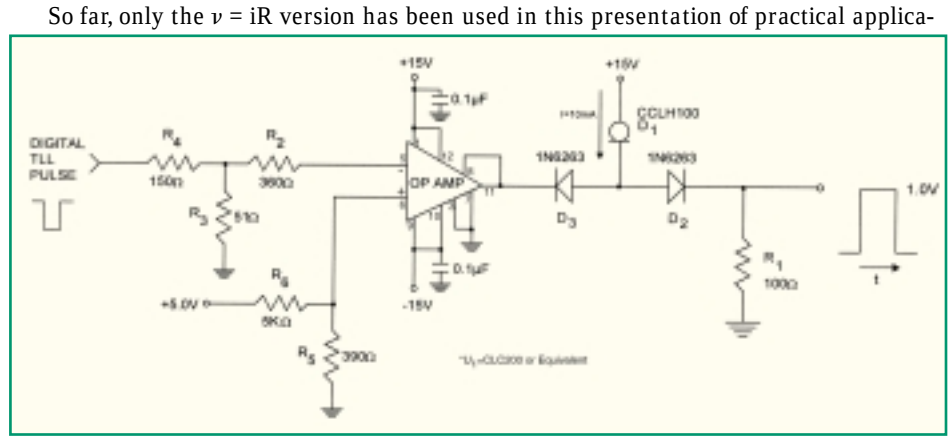

Fig. 12. Ultra High speed Pulse Amplitude Reference.
***Editor's Note*: opamp preceeds U_1=CL200 or Equivalent.**

From i = c dv/dt, if i is constant, then v is a ramp function. This means that if a constant current is switched into a capacitor, as shown in Fig. 13a, a ramp voltage which increases linearly with time is generated, as shown in Figure 13b.

If the switch is added across the capacitor as shown in Fig. 14a, and the switch is closed for some period, then opened for some other period, the output, V_C, shown in Fig. 14b is a sawtooth waveform whose shape depends on the closed and open periods of the switch.

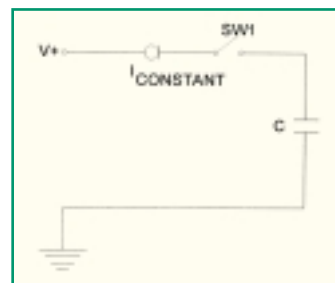

Fig. 13a. Ramp Circuit

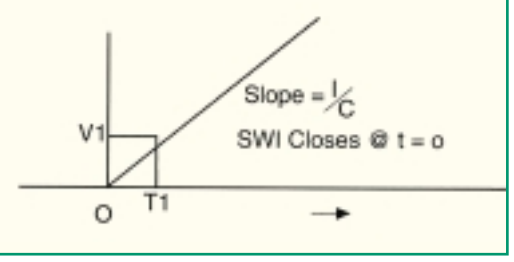

Fig. 13b. Ramp Function

Assume that the switch is closed for a very short period, then opened for a fixed period, and that this process is repeated indefinitely. The result would be a continuous sawtooth with constant peak amplitude as shown in Fig. 14c.

Application of Ramp Waveforms

It is not enough simply to know how to generate such waveforms; we must know how to apply them. Since the equation, v_C = it, relates voltage to time, one can either use its voltage characteristics to control time, or its time characteristics to control voltage.

Automatic On/Off Time (T on/T off) Detection

The ramp function of Fig. 13b may be used for automatic Ton/Toff detection. Since Ton/Toff is an important semiconductor parameter, the ability to test it automatically

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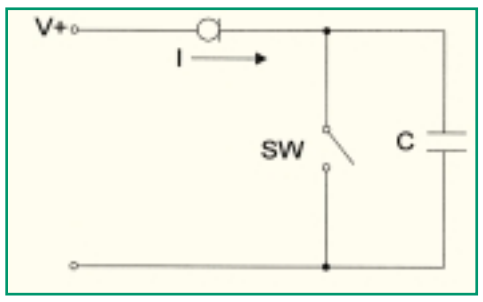

Fig. 14a. Sawtooth Circuit

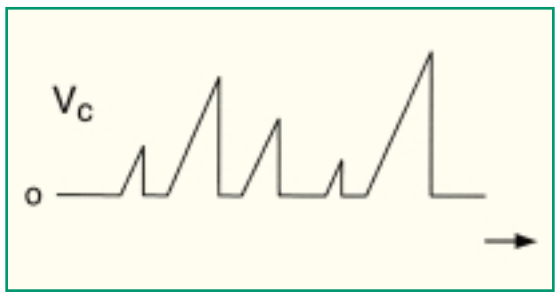

Fig. 14b. V_C = 0 when SW closed, V_C > 0 when SW open

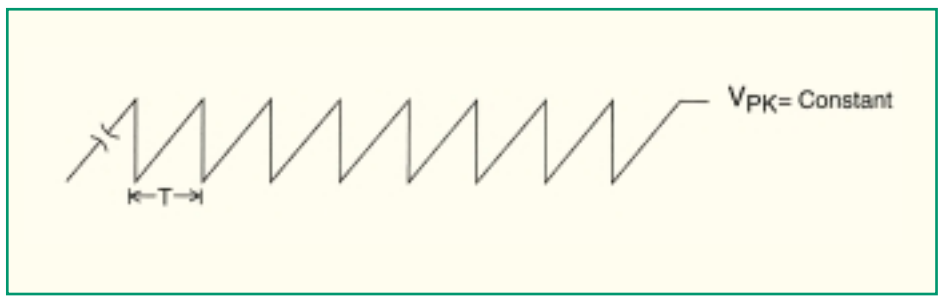

Fig. 14c. Sawtooth waveform with constant period, T, and constant V_{pk}.

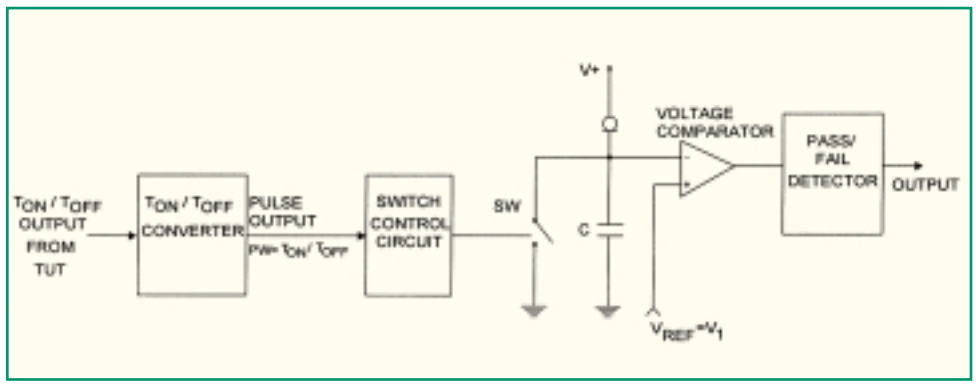

Fig. 15. Automatic T_{on}/T_{off} Detection

Shown in Fig. 16a is a simple pulse width modulator (PWM), with output waveforms for two DC signal levels shown in Fig. 16b.

This pulse width modulator may be used as part of any feedback loop to control the proper function of an electronic apparatus such as a servo amplifier, switching regulator, phase controller, or a voltage-controlled oscillator.

Using a switching regulator as an example, its DC output is proportional to the duty cycle of the switching device that chops its DC input signal. When its DC output is compared with a reference sawtooth through a pulse width modulator, the pulse width of the PWM will vary in such a way that the DC output is maintained within its accuracy range. Shown in Fig. 17 is a simplified sketch of a PWM used within a switching regulator.

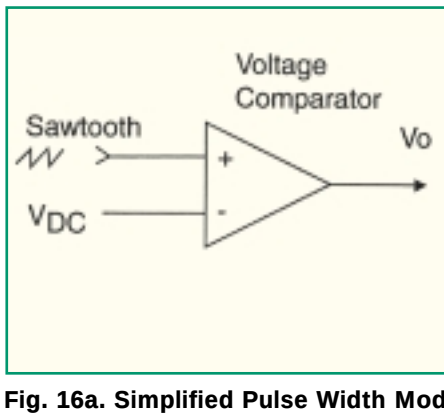

Fig. 16a. Simplified Pulse Width Modulator

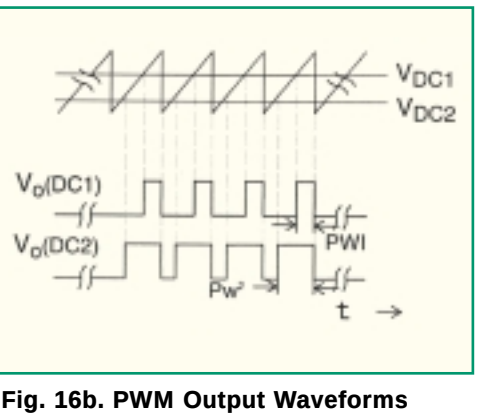

Fig. 16b. PWM Output Waveforms

Staircase Generator

A staircase waveform may be generated through the use of a sample and hold technique as shown in Fig. 18a. If various levels along the ramp are sampled and held, a staircase waveform is generated as shown in Fig. 18b. The length of each step depends on the droop rate of the sample and hold amplifier. Using a Burr Brown SHC5320 device as an example, with a droop rate of ±0.5mv/mSec max, output voltage range of ±10 V, and acquisition time of 1.5 µS max, a staircase waveform is generated that can be used for voltage level control or discrimination.

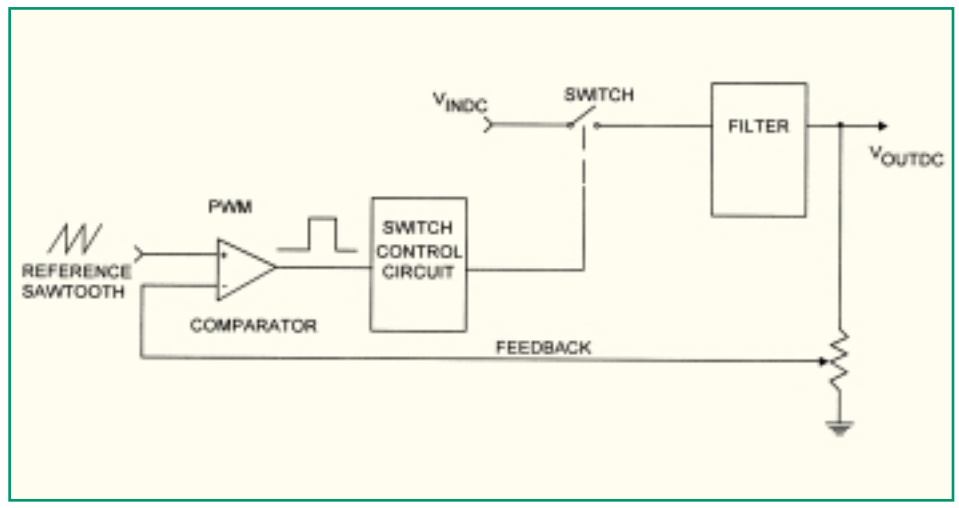

Fig. 17. Simplified Switching Regulator Circuit

Pulse Width Modulation

When a sawtooth or triangular signal is compared with a DC signal, a pulse signal may be generated. The pulse width, PW, may be varied or modulated if the level of the DC signal is varied.

Conclusion

The Current Limiting Diode, offering simplicity and high performance characteristics when compared with a bipolar transistor, has been shown to offer versatility in many circuit applications, as well as superior performance regarding temperature drift and dynamic impedance.

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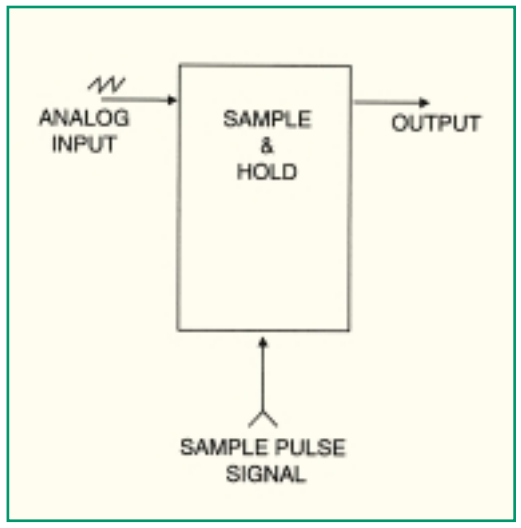

Fig. 18a. Staircase Generator Circuit

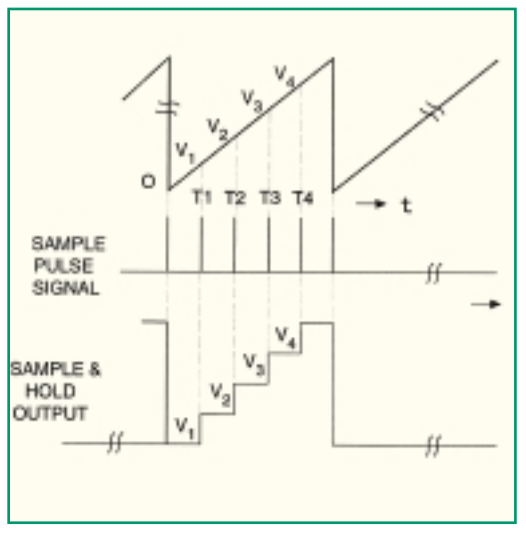

Fig. 18b. Sample & Hold Output Waveform

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